CLAIMS

Sub B1

1. A circuit for processing integer data, for graphic or image processing applications, comprising:

- a multiplier unit for multiplying integer data words, of 8 bits or multiples thereof in which unit a pipeline forms part and the word length of which is adjustable for the multiplication to be performed in accordance with the multiple of 8 bits for multiplying;

- an arithmetic logic unit (ALU) for performing arithmetic operations on integer data words of 8 bits or multiples thereof, the word length of which is adjustable in accordance with the multiple of 8 bits for processing;

- a register unit provided with at least two registers for storage therein for some time of integer data words of a multiple of 8 bits on which the operation and/or pipeline multiplication has to be performed; and

- a bus structure which comprises a number of separate buses and which effects the transport of integer data words from and to the multiplier unit, the arithmetic logic unit and the register unit.

2. A circuit according to claim 1, wherein the pipeline is a five-step pipeline.

3. A circuit according to claim 1 ~~or 2~~, wherein the integer data comprises 32 bit or 16 bit words.

4. A multiplier unit with pipeline, the word length of which is adjustable for the multiplication to be performed in accordance with the length of the integer data words for multiplying, of 8 bits or a multiple thereof.

5. An arithmetic logic unit the word length of which is adjustable in accordance with the length of the integer data words for processing of 8 bits words or multiples thereof.

6. A shift register unit for shifting a 32 bit integer data word through a distance of 1 to 32 bits to the left or the right, in rotating or non-rotating manner.

7. The circuit according to claim 1, ~~2 or 3~~, in integrated form.

8. A circuit as claimed in claim 1, ~~2, 3 or 7,~~ wherein the bus structure is provided with a number of registers or other connections and wherein these connections are programmable from an instruction register.